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DESIGN OF N×N REVERSIBLE MULTIPLIER USING MKG GATE

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ABSTRACT

Every system performance depends on low power consumption and smaller area .Optimizing the speed and area in the multiplier is the major design issues. For providing better solution for those issues by using reversible logic design. Reversible logic is emerged as the promising technology having its application in low power CMOS, This paper proposes a NXN reversible multiplier using MKG gate. It is based on two concepts. The partial products can be generated in parallel with a delay of d using Fredkin gates and thereafter the addition can be reduced to log2N steps by using reversible parallel adder designed from MKG gates. Similar multiplier architecture in conventional arithmetic (using conventional logic) has been reported in existing literature, but the proposed one in this paper is totally based on reversible logic and reversible cells as its building block. A 4x4 architecture of the proposed reversible multiplier is also designed. It is demonstrated that the proposed multiplier architecture using the MKG gate is much better and optimized, compared to its existing counterparts in literature; in terms of number of reversible gates and garbage outputs. Thus, this paper provides the initial threshold to building of more complex system which can execute more complicated operations using reversible logic.

***Index Terms*—**garbage output,gate count,constant input,power consumption.

1. INTRODUCTION

Definitions

Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Furthermore, voltage-coded logic signals have energy of Esig = ½CV2, and this energy gets dissipated whenever switching occurs in conventional (irreversible) logic implemented in modern CMOS technology. It has been shown that reversible logic helps in saving this energy using charge recovery process [13]. Reversible circuits are those circuits that do not lose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors.
Thus, an NXN reversible gate can be represented as
Iv=(I1,I2,I3,I4,……IN)
Ov=(O1,O2,O3,……ON).
Where Iv and Ov represent the input and output vectors respectively. Classical logic gates are irreversible since input vector states cannot be uniquely reconstructed from the output vector states. There are a number of existing reversible gates such as Fredkin gate[3,4,5], Toffoli Gate (TG) [3, 4] and New Gate (NG) [6].

Motivation behind Reversible Logic

The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low power CMOS design, optical computing, quantum computing and nanotechnology. The most prominent application of reversible logic

lies in quantum computers. A quantum computer can be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performs an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible, hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, Quantum Arithmetic must be built from reversible logic components [10].

Proposed Contribution

In this paper, the focus is on the application of new reversible 4*4 MKG gate [12] and its implementation for designing novel reversible multiplier. A NXN reversible multiplier is also proposed in this paper. A similar multiplier in conventional arithmetic (using conventional logic) has been reported in [14]. It is based on two concepts. The partial products can be generated in parallel with a delay of using Fredkin gates and thereafter the addition can be reduced to log2N steps by using reversible parallel adder designed from MKG gates. A 4x4 architecture of the proposed reversible multiplier is also designed. It has been proved that the proposed multiplier architecture using the proposed MKG gate is better than the existing ones in literature, in terms of number of reversible gates and garbage outputs. The reversible circuits designed and proposed in this paper form the basis of the ALU of a primitive quantum CPU.

2. REVERSIBLE LOGIC GATES

An nxn reversible logic gate can be represented as:
IV = (I1, I2, I2,…,IN)
OV = (O1, O2, O3,…,ON)
Where Iv and Ov are input and output vectors respectively. Several reversible logic gates have been proposed in the past few decades. Some of them are: Feynman gate, FG [6], Toffoli gate, TG [7], Fredkin gate, FRG[15], Peres gate, PG [11], New Gate, NG [14], TSG gate, TSG [5], MKG gate, MKG [16] and HNG gate, HNG [18]. In this section we review these reversible logic gates. Some of them are presented to allow for comparison with existing studies.

Feynman gate (FG)

Feynman gate (FG), also known as controlled-not gate (1-CNOT), is a 2×2 gate that can be described by the equations:

Iv = (A, B)

Ov = (P = B, Q = A ⊕ B)

where 'A' is control bit and 'B' is the data bit. It is shown in Fig. 1.

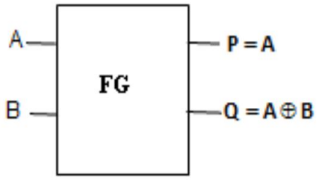

Figure1 Feynman Gate

Fredkin gate (FRG)

Fredkin gate (FRG), also known as controlled permutation gate, is a 3x3 reversible logic gate. It can be represented as:

Iv = (A, B, C)

Ov = (P = A, Q = A′B⊕AC, R = A′C⊕AB)

Where Iv and Ov are input and output vectors.
It is shown in Fig. 2. Fredkin Gate is a conservative gate, that is, the Hamming weight of its input vector is the same as the Hamming weight of its output vector.

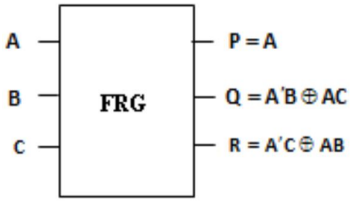

Figure 2 Fredkin Gate

Toffoli gate (TG)

Toffoli gate (TG), also known as controlled controlled-not (CCNOT), is a 3x3 reversible logic gate. The Toffoli gate can be represented as:
Iv = (A, B, C)
Ov = (P = A, Q = B, R = AB⊕C)
Where Iv and Ov are input and output vectors. The Toffoli gate is shown in Fig. 3.

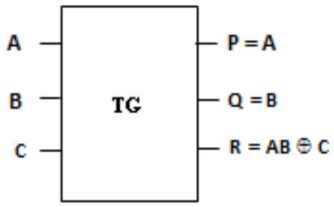

Figure 3.Toffoli Gate

Peres gate (PG)

Peres gate (PG), also known as New Toffoli Gate(NTG), combining Toffoli gate and Feynman gate is a 3x3 reversible logic gate. It can be represented as:
Iv = (A, B, C)
Ov = (P = A, Q = A⊕B, R = AB⊕C)

Where Iv and Ov are the input and output vectors. The Peres gate is shown in Fig. 4. Peres gate is equal with the transformation produced by a Toffoli Gate followed by a Feynman Gate.

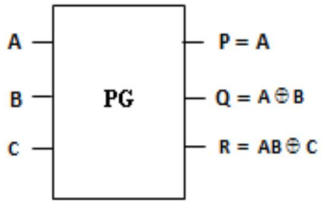

Figure 4.Peres Gate

New gate (NG)

New gate (NG), is a 3x3 reversible gate. It can be represented as

Iv = (A, B, C)

Ov = (P = A, Q = AB⊕C, R = A′C′⊕B′)

Where Iv and Ov are the input and output vectors. The New gate is shown in Fig. 5.

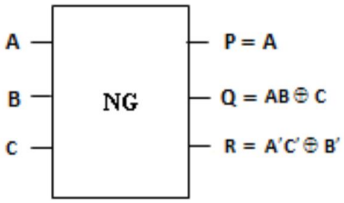

Figure 5New Gate

TSG gate

TSG gate is a 4×4 reversible gate. The TSG gate is shown in Fig. 6., where each output is annotated with the corresponding logic expression:

Iv = (A, B, C, D)

Ov = (P = A, Q = A′C′ ⊕ B, R = (A′C′⊕ B′)⊕ D, S = (A′C′⊕ B′) D ⊕ (AB⊕C))

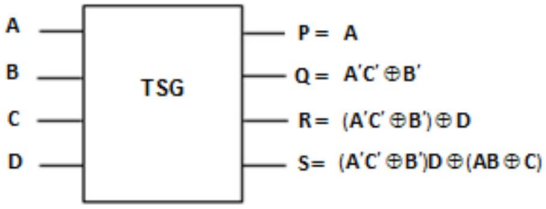

Figure 6.TSG gate

HNG gate

The HNG gate is universal. The HNG gate is shown in Fig.8., where each output is annotated with the corresponding logic expression. The corresponding logic expression of HNG gate:

Iv = (A, B, C, D)

Ov = (P = A, Q = B, R = A⊕B⊕C,

S = (A⊕B).C⊕AB⊕D)

Figure 7 HNG gate

3. PROPOSED 4* 4 REVERSIBLE GATE

Here 4*4 through reversible gate called MK gate (MKG) [12] which is shown in Figure 1. It can be verified that the input pattern corresponding to a particular output pattern can be uniquely determined. The proposed MKG gate is capable of implementing all Boolean functions and can also work singly as a reversible Full adder. Figure 2 shows the implementation of the proposed gate as a reversible Full adder

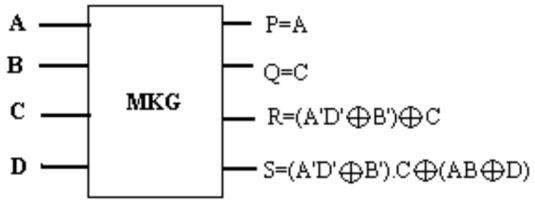

Figure 8 MKG Gate

A number of reversible full adders were proposed in [6,7,8,9]. The reversible full adder circuit in [6] requires three reversible gates (two 3*3 new gates and one 2*2 Feynman gate) and produces three garbage outputs (garbage output refers to the output that is not used for further computations. In other words, it is not used as a primary output or as an input to other gate). The reversible full adder circuit in [7,8] requires three reversible gates (one 3*3 new gate, one 3*3 Toffoli gate and one 2*2 Feynman gate) and produces two garbage outputs. The design in [9] requires five reversible Fredkin gates and produces five garbage outputs.

The proposed full adder using MKG in Figure 8 requires only one reversible gate (one MKG gate) and produces only two garbage outputs. Hence, the full-adder design using MKG gate is better than the previous full-adder designs of [6,7,8,9]. A comparison of various full adders is shown in Table 1.

Table 1. Comparison of Various Reversible Full Adder Circuits

	Number of Gates	Number of Garbage Output	Unit Delay
Proposed System	1	2	1
Existing System[6]	3	3	3
Existing System[7,8]	3	2	3
Existing System[9]	5	5	5

Novel Reversible Multiplier Architecture

The proposed reversible NXN bit parallel multiplier architecture is an improvement over reversible array multiplier [11]. Similar multiplier architecture in conventional arithmetic (logic) has been reported in [14], but the proposed one in this paper is totally based on reversible logic and reversible cells as its building block. It is based on two concepts.

The partial products can be generated in parallel with a delay of d using Fredkin gates and thereafter the addition can be reduced to log2N steps by using reversible parallel adder designed from MKG gates. Each two adjacent partial products will be added together with an N-bit reversible parallel adder. A number of interesting and optimized parallel adders are proposed in [12].

The addition of adjacent partial products will generate the first level of computation with N/2 partial sums. These partial sums are added again in the aforesaid fashion to create a second level of computation with N/4 partial sums. The final product will be obtained at the log2N level. The working of the multiplier can be deeply understand by considering a binary tree having N leaf nodes (equivalent to N partial sums) which are merged to form their N/2 parents (equivalent to N/2 Partial Sums). These N/2 parents are again added in the aforesaid fashion and finally this process will be successively repeated to the get at the root of the tree(final product). Thus, the required number of levels to compute the multiplication result will be log2N.

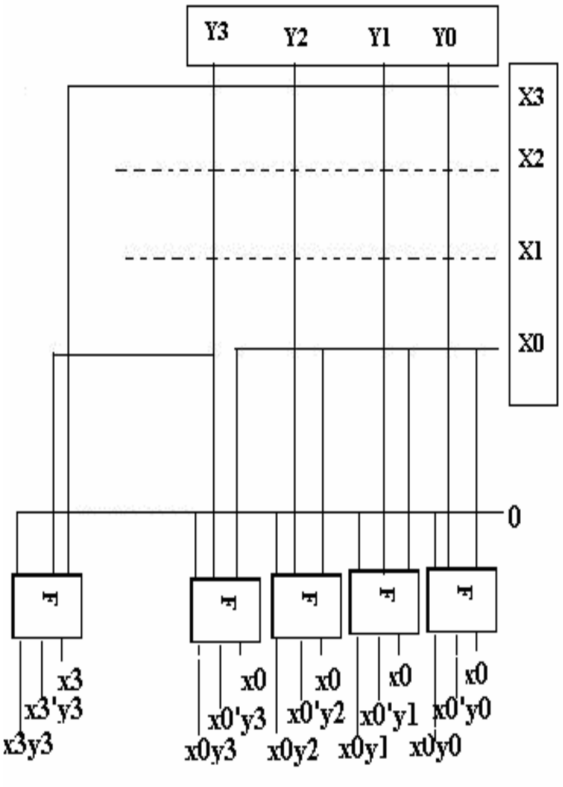

Figure 9. Parallel generation of Partial Products using Fredkin Gates

ince this architecture requires (N-1) of N-bit reversible adders, it needs a total of N *(N-1) reversible full adder cells. So, the worst propagation delay of the proposed multiplier architecture can be computed as: - d+N*d'[log2N] where d and d' are the propagation delays of a Fredkin gate and reversible MKG gate (adder) respectively. By changing the type of adder such as reversible CLA (Carry Look Ahead Adder) to reversible CPA (Carry Propagate Adder) will make a substantial change in the propagation delay. The proposed NXN reversible multiplier is designed for 4x4 bit. In the 4x4 multiplier, the partial products are generated in parallel using Fredkin gates as shown in Figure 3. Thus, we have 4 partial products generated as shown in Figure 4. Each 2 partial products are added using 4-bit reversible parallel adder creating the first level of computation which has 2 partial sums. These two partial sums are fed to the second level of 4-bit reversible parallel adder, resulting in the formation of the final product. The proposed reversible multiplier efficiency significantly depends on the type of reversible parallel adders used in addition operation. The proposed reversible multiplier is shown in Figure 5 for 4x4 bit. The multiplier uses the proposed MKG gates as reversible full adder units.

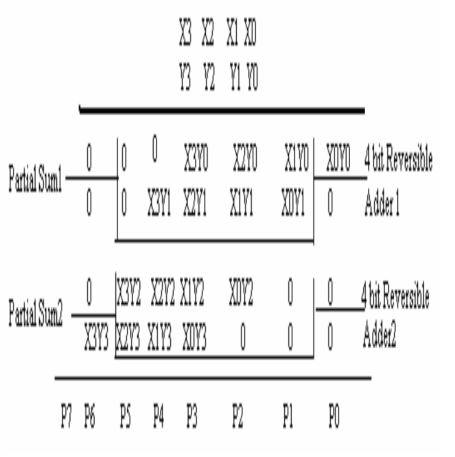

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Figure 10. Methodology of 4x4 reversible Multiplier

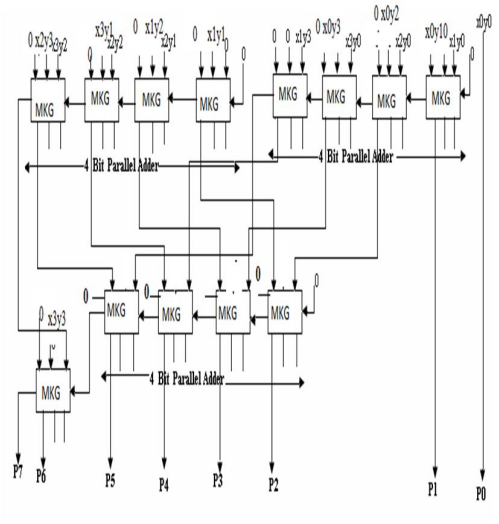

Figure 11 . Proposed 4 x4 Novel Reversible Multiplier

Evaluation Of The Proposed Reversible Multiplier

The efficiency of the proposed reversible multiplier greatly depends on the choice of the reversible parallel adder. The efficient parallel adders proposed in [12] will significantly improve the multiplier efficiency. The proposed architecture can further be optimized through a control circuitry. As we have decomposed all the operations into levels, we can significantly reduce the power consumption by employing a control circuitry which will switch off those levels which have done their computations. Therefore, switching off the levels as the computations proceed in the multiplier will lead to a great reduction in power consumption. Furthermore, the multiplier can be optimized for power by having leading zeroes count for both the multiplicand and the multiplier, thus reducing the power consumption by running less number of adders and switching off those adders which are not in use. The multiplier is most optimized compared to its existing reversible counterpart in literature [11]. The proposed 4x4 bit multiplier is designed with bare minimum of 29 reversible gates while its existing counterpart in [11] has 40 reversible gates. The results can be generalized for NXN bits. The numbers of garbage outputs are nearly same for both the multiplier.

4. CONCLUSIONS

The focus of this paper is the application of the recently proposed reversible 4*4 MKG gate. A NXN reversible multiplier is also proposed in this paper. It is proved that the proposed multiplier architecture using the proposed MKG gate is better than the existing counterpart in literature in terms of reversible gates and garbage outputs. All the proposed architectures are analyzed in terms of technology independent implementations. The technology independent analysis is necessary since quantum or optical logic implementations are not available. There are a number of significant applications of reversible logics such as low power CMOS, quantum computing, nanotechnology, and optical computing and the proposed MKG gate and efficient multiplier architecture are one of the contributions to reversible logic. The proposed circuit can be used for designing large reversible systems. In a nutshell, the advent of reversible logic has contributed significantly in reducing the power consumption. Thus, the paper provides the initial threshold to build more complex systems which can which can execute more complicated operations. The reversible circuits designed and proposed here form the basis of the ALU of a primitive quantum CPU.

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